B.E. / B.Tech. Electrical (Electronics & Power) Engineering (Model Curriculum) Semester-IV

SE202 - Digital Electronics

P. Pages : 2 **GUG/S/25/13804**

Time : Three Hours Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Assume suitable data wherever necessary.
3. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Convert (1010011011110001) into hexadecimal and octal. **4**

b) Compute the 1's complement form of (-43) and (+25) **4**

c) What do you mean by self-complementing codes? Explain with an example. **4**

d) Convert **4**
i) 1110 from Gray to decimal.
ii) Decimal 14 to gray code.

OR

2. a) Represent the decimal numbers 535 in BCD and Excess-3. **4**

b) Find the 9's and 10's complement of 110. **4**

c) Derive the 6-bit sign-magnitude, 1's complement, and 2's complement of the following decimal numbers: **8**
i) +22 ii) -31
iii) +17 iv) -8

3. a) Find the dual of the following Boolean functions **4**
$f(a,b,c) = \bar{a}\bar{b}c + b\bar{c} + ac$

b) A combinational circuit has 3 outputs F1, F2 and F3: **8**
$F1 = x'y'z' + xz$
$F2 = xy'z' + x'y$
$F3 = x'y'z + xy$
Design the circuit with a decoder and external gates.

c) Realize half adder using 2:1 mux. **4**

OR

4. a) Simplify the following expression using consensus law. **4**
$(\bar{x} + y)wz + x\bar{y}v + vwz$

b) Convert the following Boolean functions into **6**
i) $f(X,Y,Z) = XY + X\bar{Z} + YZ$ canonical standard SOP form
ii) $f(X,Y,Z) = (X+Y)(\bar{X}+Z)$ canonical standard POS form

c) Draw NOT gate, AND gate and OR gate using NAND gates only. **6**

5. a) Explain the operation of SR latch using. **8**
i) NAND gates only
ii) NOR gates only
Also write their truth table.

b) Explain Johnsons counter with the help of diagram and truth table. **8**

OR

6. a) Explain SISO and SIPO shift register. **6**

b) Design a 3-bit up-down synchronous counter with direction control M. When M = 0 the counter counts upward and M = 1 the counter counts downward (Assume JK Flip Flop). **10**

7. a) Explain following specification of DAC: **8**
i) Resolution
ii) Full scale voltage
iii) % Resolution
iv) Accuracy.

b) Explain Dual slope A/D converter with neat diagram. What is its maximum conversion time? **8**

OR

8. a) Draw the diagram of counter type A/D converter. Also explain its operation. **8**

b) Define DAC? Write few applications of DAC. **4**

c) An eight-bit D/A converter has a step size of 20 mV. Determine the full-scale output and percentage resolution. **4**

9. a) Show that logic arrangement of both a PROM and a PLA required to implement a binary full adder. **8**

b) Draw the architecture of CPLD. Compare CPLD and FPGA. **8**

OR

10. a) Implement 4-bit Binary to gray code convertor using ROM. **8**

b) Write short note on **8**
a) CCD b) CAM

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